A Fully Integrated, Single-Chip Handset Power Amplifier in SiGe BiCMOS for W-CDMA Applications

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Abstract — **A fully integrated, single-chip power amplifier has been designed to meet the requirements of W-CDMA mobile handsets. The circuit was designed in IBM's 47 GHz f_T SiGe BiCMOS process with all passive components and matching circuits included on-chip. The design achieves 24 dBm output power with 30% PAE and excellent linearity. The power amplifier draws 42 mA of quiescent current from a 3.3 V source. The fabricated circuit occupies a die area of 1.8 mm x 1.25 mm, offering at least 10x improvement in chip/board area over current designs, allowing for increased levels of transmitter integration.**

I. Introduction

SiGe BiCMOS technology has emerged as a competitor to III-V technologies for use in handset power amplifiers (PA's) due to the potential integration it offers with other transceiver components. Other research reports on SiGe PA deigns that meet the specifications of several current wireless communications standards [1]-[3]. Those circuits follow the traditional power amplifier design methodology using board or package level lumped elements or transmission lines for impedance matching, filtering, and harmonic suppression. This approach is currently favored because it allows a wide range of post-fabrication tuning of circuit performance. However, this tuning ability comes at a sacrifice in design time, cost, bill of materials, and module/board area. Extensive use of on-chip passive components has been avoided in most circumstances because of the low quality factors (Q) of integrated components, particularly on silicon substrates.

Commercial foundry processes such as IBM's SiGe 5AM process offer back-end-of-line advances that provide reasonably high Q-factors for on-chip capacitors and inductors. The SiGe 5AM process uses a 4μm thick analog metal layer to create inductors with peak Q approaching 20 [4]. With these improved passive components, much work has already been done to integrate entire receiver and transmitter circuits as single-chip designs. These transmitter designs still rely on separate power amplifier chips with their own off-chip passive elements, which presents an obstacle to the realization of a single-chip transceiver [5]-[6].

This work presents a circuit that utilizes the on-chip passive components of the SiGe 5AM process to provide a fully integrated, single-chip power amplifier for W-CDMA handsets. The target design goals are based on the 3GPP W-CDMA specifications, listed in Table 1 [7]. To our knowledge, this is the first entirely single-chip power amplifier that meets the needs of this modern communications system.

TABLE I
3GPP W-CDMA Power Amplifier Specifications

Specification	Value
Frequency Range	1.92 – 1.98 GHz
Max. Output Power	+24 dBm (power class 3)
Linearity (ACPR)	-33 dBc @ 5MHz offset -43 dBc @ 10 MHz offset
Power Added Efficiency	≥30%

II. Design Approach

The power amplifier is a two-stage design with all matching components integrated on-chip. A simplified circuit schematic is shown in Fig. 1. The PA uses SiGe HBT's with a breakdown voltage of 5.5V and an f_T of 27 GHz. For best performance it is desired to operate the devices near the peak f_T value, but this results in current densities that are too high for reliable operation. As a tradeoff, the emitter areas of the output stage and driver stage transistors are optimized to provide the maximum f_T

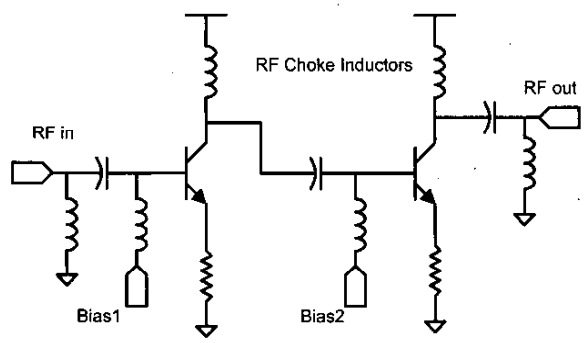

Fig. 1. Simplified power amplifier schematic

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for acceptable device current densities. The total emitter areas of the driver and output stage transistors are chosen to be 400μm^2 and 1200μm^2, respectively.

At high current levels, the heat dissipated by the HBT's can create positive thermal-electric feedback. Due to resistive losses and current distributions, this can be very localized to one or a few devices. These local hot spots can lead to breakdown in the form of thermal runaway. Emitter ballasting is employed to prevent this thermal runaway in large signal operation [8]. The emitter ballasting resistors help distribute the current evenly between the emitter fingers of the devices to limit thermal differences between transistors. Both the driver and the output stage use 4Ω resistors in series with every pair of 10μm^2 emitter fingers. Because of the large number of emitter fingers in both the driver and output stage transistor cells, the parallel resistance in the emitter is very small and has a minimal effect on the output voltage swing of each device.

The driver stage is biased for deep Class-AB operation, while the output stage operates as a normal Class-AB amplifier to minimize power consumption while maintaining high linearity. The driver stage class of operation was chosen to improve the linearity of the circuit further by providing gain expansion at high input power [9]. This counteracts the gain compression of the output stage, providing a larger linear operating range. For the initial design, biasing is provided by the test setup.

The matching networks are pi-networks that incorporate the bias choke inductors into the impedance match. A high-pass topology was required because of the lower Q-factor of the on-chip inductors, which results in signal losses if used in a low-pass configuration. This is a limitation because low-pass networks provide some harmonic filtering of the signal. The high linearity of the SiGe HBT devices provides sufficient design headroom to allow the use of on-chip matching and still meet the required linearity specifications. Despite the reduced linearity, the overall goal of full integration makes this design concession acceptable.

As mentioned previously, the power amplifier is designed to operate in the 1.92 – 1.98 GHz W-CDMA transmit band in power class 3 (24 dBm output power). Based on these specifications, the output match was initially determined using the Cripps method to calculate the optimal real impedance required to provide the desired output power [10]:

$$R_{opt} = \frac{V_{DC}}{I_{fund}} \qquad (1)$$

$$P_{opt} = \frac{V_{DC} I_{fund}}{2} \qquad (2)$$

where I_{fund} is the fundamental frequency current component from Fourier analysis. The Fourier component is necessary because of the reduced conduction angle of the signal resulting from class AB to class B operation. If the amplifier were operated in class A, I_{fund} would be equivalent to I_{DC}. Combining (1) and (2) and including the HBT saturation voltage gives a calculation of R_{opt} based on the desired output power:

$$R_{opt} = \frac{(V_{DC} - V_{CEsat})^2}{2P_{opt}} \qquad (3)$$

An additional design concern with a fully integrated approach is the parasitic resistance of the output stage choke inductor. Due to the resistance in the inductor, the collector voltage drops by several millivolts at maximum RF output power. Taking this effect into account, the impedance value seen by the output stage and calculated from (3) has to be decreased to provide maximum power transfer as shown below:

$$R_{opt} = \frac{(V_{DC} - V_{CEsat} - R_{ind} I_{DC\max})^2}{2P_{opt}} \qquad (4)$$

Once the real component of the impedance value is calculated from (4), a large signal load-pull simulation is performed on the extracted layout netlist (including layout parasitics) using Xpedion's Golden Gate software to determine the overall output impedance of the power amplifier. Adjusting the output matching network compensates for the reactive component of the PA output impedance and provides a purely resistive impedance termination. Attention is given to the layout of the power amplifier in order to minimize the inductive parasitics of the large collector and emitter metallization.

III. RESULTS

The power amplifier occupies 1.8mm x 1.25 mm of die area, including the bias and probing pads. This demonstrates the size advantage of full integration. A die photograph of the fabricated power amplifier is given in Fig. 2. Comparable commercially available MMIC or packaged power amplifiers require almost 10 times the board area of this design. Multiple bonding pads are provided for supply voltage and ground to ensure good test performance. Due to the choice of class of operation for the PA, the circuit only consumes 42 mA of quiescent current from a 3.3 V supply.

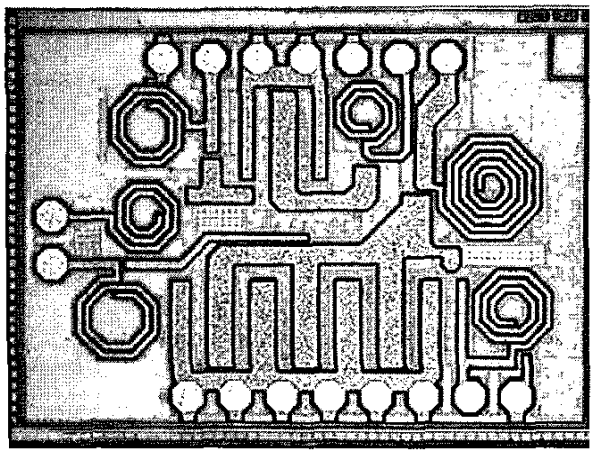

Fig. 2. Microphotograph of fabricated power amplifier

S-parameter simulated and measured results for the power amplifier are shown in Fig. 3. The small signal gain S_{21} is 24 dB at center-band and varies less than 1.0 dB across the frequency band of operation. The measured input return loss S_{11} is less than –20 dB, and the measured output return loss S_{22} never exceeds –9 dB, limiting the VSWR at the input and output of the PA. Based on harmonic balance simulation of the circuit including extracted layout parasitics, the power amplifier achieves +24 dBm output power with a PAE of 30% at 1.95 GHz, as shown in Fig. 4.

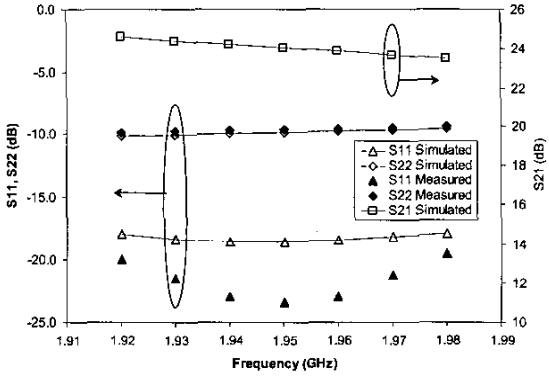

Fig. 3. Simulated and measured s-parameters for W-CDMA transmit frequency band

Simulation of large signal circuit behavior with an actual W-CDMA waveform was possible using Xpedion's GoldenGate software add-in for Cadence. Using the fast envelope simulation, the adjacent channel power ratio (ACPR) was simulated for 5 and 10 MHz offsets from the channel. Fig. 5 gives the linearity performance of the circuit, demonstrating an ACPR of 30.7 dBc at 5 MHz offset and 41.3 dBc at 10 MHz offset for +24 dBm output power. While slightly below the W-CDMA specifications, the fast envelope simulation used gives a pessimistic value for ACPR, often 1-3 dB worse than actual values [11]. The effect of the gain expansion due to the biasing of the driver stage can be seen in Fig. 5 as the flattening of the ACPR curves between –10 dBm and –4 dBm input power. This gain expansion technique extends the linear range several dB compared to a flat driver gain characteristic.

Further measurements were not possible due to oscillation conditions involved with the biasing of the power amplifier. Oscillation may be due to parasitic resonances in the matching networks or improper terminations of the DC bias inputs. This prevented both stages from being biased to the proper DC operating point simultaneously, resulting in the inability to extract proper small signal gain and large signal performance.

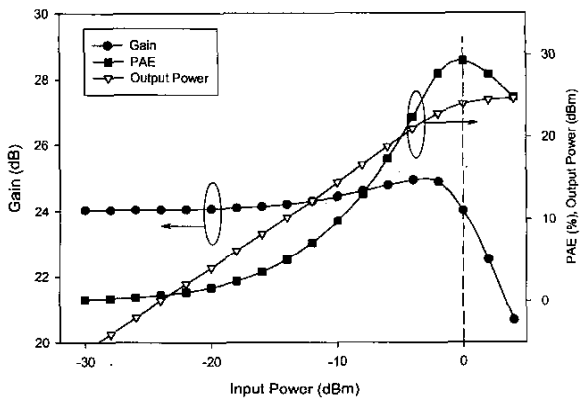

Fig. 4. Simulated gain, output power, and power added efficiency (PAE) at 1.95 GHz

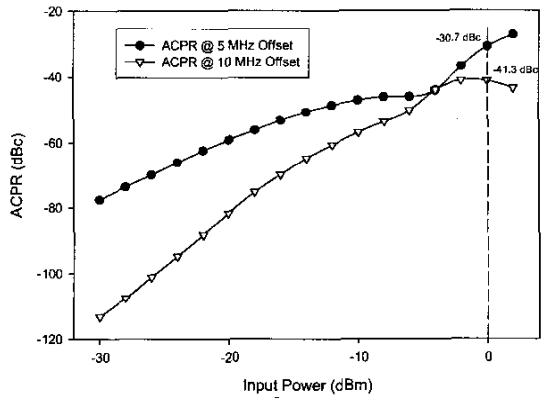

Fig. 5. Simulated ACPR at 1.95 GHz for 5, 10 MHz offset

IV. Conclusion

A fully integrated power amplifier that includes all matching components on a single chip is presented for use in W-CDMA handsets. The design achieves simulated results of +24 dBm output power with 30% PAE and good linearity. Due to oscillation of the circuit when DC bias was applied, full circuit performance could not be evaluated. However, the measured values of input and output return loss S_{11} and S_{22} indicate that the matching network values closely match those from simulation. This leads the authors to believe that if the oscillation could be suppressed, the circuit performance would agree with the simulated results. Despite this oscillation, the design demonstrates that a fully integrated, single-chip power amplifier approach is not beyond the reach of current technologies. Such an integrated power amplifier enables the realization of a single-chip transceiver for wireless handset applications. Additionally, the use of a SiGe BiCMOS technology allows the integration of more complex efficiency and linearity control circuitry directly on chip to improve the power amplifier performance through adaptive techniques.

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